Main Memory

Review Questions

Section 9.1

9.1 What two registers can be used to provide a simple form of memory protection?

9.2 List the three different times at which address binding may occur.

9.3 True or False? An address generated by the CPU is also referred to as a physical address.

9.4 What is the hardware device that maps virtual to physical addresses?

Section 9.2

9.5 What are the three strategies for selecting a free hole from the set of available holes?

9.6 What are the two forms of fragmentation?

Section 9.3

9.7 What are the two parts of an address generated by the CPU?

9.8 What does each entry in the page table contain?

9.9 True or False? Fragmentation can still occur in paging systems.

9.10 What is the term that describes when a page number is not present in the TLB?

Section 9.4

9.11 If a page offset is 13 bits, how large (in bytes) is the page?

9.12 How many entries are in a two-level page table with a 20-bit page number?

9.13 What is an alternative to hierarchical paging for large (> 32 bits) address sizes?

Section 9.6

9.14 True or False? IA-32 address translation involves both paging and segmentation.

9.15 True or False? In practice, all 64 bits are used with IA-64 addressing.

Section 9.7

9.16 What are the three components of a 32-bit ARM address?